REMARKS

Claims 1-24 are pending in this application, of which claims 1, 11, 19, and 20 are independent. Claims 1-3, 7, 11, and 16-20 have been rejected, and claims 4-6, 8-10, and 12-15 have been objected to based on dependency. Claims 1, 11, 19, and 20 have been amended and claims 21-24 have been added. Care has been taken to avoid the introduction of new matter. Favorable reconsideration is respectfully solicited.

Examiner's Interview

The Examiner is thanked for the courtesy extended during the Examiner's Interview of December 9, 2002. The novel features of claims 1, 11, 19, and 20 (before amendment) discussed herein memorialize the positions set forth during the interview.

Claim Rejections and Objections

Claims 1-3, 7, and 19 stand rejected under 35 U.S.C. §102(e) as being anticipated by Crotty, and claims 11, 16-18, and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Crotty. The Office Action objects to claims 4-6, 8-10, and 12-15 as being dependent upon a rejected base claim, but indicates that the claims would be allowable if rewritten in independent form incorporating limitations of the base claim and any intervening claim. Applicants respectfully traverse.

Claim Amendments

Amendments to the claims incorporated herein amplify novel features disclosed by the present application, which include the ability to detect a voltage level independently of another voltage level.

Prior Art Analysis and Independent Claims 1, 11, 19, and 20

Crotty discloses in Fig. 6 a power-on detection circuit including dual voltage detection circuit 210 for generating a first voltage level detection signal VD1 having a voltage level determined according to the first power supply voltage Vcc1 *only* when the second power supply voltage Vcc2 is in a steady state. This is because the voltage detection signal VD1 is driven by circuitry powered by the second power supply Vcc2, and therefore, must be at a steady state to generate the first voltage level detection signal VD1. (*See col. 2, lines 45-55*). A second voltage level detection circuit 630 detects a voltage level of the second power supply voltage Vcc2 to generate the second voltage level detection signal VD2. A buffer circuit 650 receiving signals POR1, POR2 corresponding to VD1 and VD2, respectively, generates the power-on detection signal POR in accordance with voltage level detection signals VD1 and VD2.

As a result, when the second power supply voltage Vcc2 is not supplied (or is at a level below adequate), the first and second power-on detection signals POR1 and POR2 are in an inactive state. (*See col. 9, lines 5-15 and lines 18-24).* Thus, the power-on detection signal POR is also in an inactive state.

Detection of Vcc1, the first power supply voltage, is completely dependent on a second power supply voltage, Vcc2. To do otherwise would be contrary to the intended purpose of Crotty. Specifically, Crotty teaches a dual voltage detector 210 for detecting Vcc1 dependent on a steady level of Vcc2 (*See col. 2, lines 45-55*) to overcome the problems of "erroneous results" when a "circuit is partly power up." (*See col. lines 24-31*).

Contrary to the teachings of Crotty, claims 1, 11, 19, and 20 require detecting power-on (or a voltage level) independently of another voltage level. Portions of claims 1, 11, 19, and 20

are recited below, with certain language underscored for emphasis, and should not be understood as limitings.

Claim 1 recites "a second power-on detection circuit...for detecting power-on of said second power supply voltage independently of a voltage level of said first power supply voltage, to activate a second power-on detection signal according to a result of detection, said first power-on detection circuit performing detection of the power-on independently of a voltage level of the second power supply voltage."

Claim 11 recites "a power-on detection circuit for detecting power-on of a second power supply voltage independently of a voltage level of said internal voltage, to activate a power-on detection signal according to a result of detection, said internal voltage application detection circuit performing detection of the voltage level of the internal voltage independently of a voltage level of the second power supply voltage."

Also, claim 19 recites "each power-up detection circuit detecting a voltage level of a corresponding power supply voltage independently of a voltage level of the power supply voltage other than the corresponding power supply voltage."

Even further, claim 20 recites "power-on detection circuitry..., for detecting power-on of said at least one power source voltage in accordance with a voltage level of said at least one power source voltage independently of the voltage level of said at least one internal voltage,..., said internal voltage power-up detection circuitry performing detection independently of the voltage level of the at least one power source voltage."

* * *

Claim 1 recites further "a main power-on detection circuit responsive to said internal voltage power-up detection signal and said power-on detection signal for generating a main

power-on detection signal rendered active from activation of a first activated detection signal of the internal voltage power-up detection signal and the power-on detection signal until inactivation of second activated detection signal of the internal voltage power-up detection signal and the power-on detection signal."

In characterizing the recited portion of claim 1 with regard to Crotty, the Office Action asserts that the buffer circuit 650 (embodied by an AND gate) operates in this regard. However, the Office Action's interpretation of Crotty is incorrect.

Specifically, dual voltage detection circuit 210 outputs an active signal VD1 *only* when both Vcc1 and Vcc2 are in a stable state. In other words, the detection of Vcc1 is dependent on a stable state of Vcc2, as Vcc2 powers the circuitry for outputting VD1. This configuration renders the buffer circuit 650 incapable of operating in accordance with the underscored claim language recited above. The following scenarios will aid with the understanding.

(1) Vcc1 Powered Up First and Vcc2 Powered Up Second

In Crotty, when the first power supply voltage Vcc1 is powered up and then the second power supply voltage Vcc2 is powered up, the power-on detection signal POR1 (or the voltage level detection signal VD1) is held in an inactive state until power up of the second power supply voltage Vcc2. Specifically, in this operation, the first power supply voltage Vcc1 is powered up earlier, and is in the stable state when the second power supply voltage is stabilized, but during this time, the signal VD1 or POR1 is held in an inactive state. To put it another way, determination on the voltage level of the first power supply voltage Vcc1 is made after power up and stabilization of the second power supply voltage Vcc2, and no determination is made on the power up of the first power supply voltage Vcc1. During this time, POR maintains an inactive state.

Meanwhile, since Vcc2 is powered up second, the power-on detection signal POR2 (or the voltage level detection signal VD2) is also held at the inactive state. Once Vcc2 reaches a stable state, both POR1 and POR2 (corresponding to VD1 and VD2, respectively) change to an active state, and so does the output signal POR of buffer 650.

In this instance, POR is rendered active from activation of both of the activation signals POR1 and POR2, which is contrary to the language of claim 1.

(2) Vcc2 Powered Up First and Vcc1 Powered Up Second

According to the configuration of Fig. 8 in Crotty, when the second power supply voltage Vcc2 is powered up, the second power-on detection signal POR2 is first held at the inactive state, and then is activated when the second power supply voltage Vcc2 is stabilized. During this time, POR is in an inactive state. Once stabilized, determination is made on the voltage level of the first power supply voltage Vcc1 to determine the state of the first power-on detection signal POR1. Once Vcc1 attains an active state, so does POR1. As a result, when both voltages are at power-on level, POR attains an active level.

Due to the voltage dependency of the dual voltage detection circuit, POR is inactive until activation of both POR1 and POR2, as described in scenario (1) and scenario (2). In the event that either of the power supply voltages, Vcc1 or Vcc2, goes from a power-on state to a power-off state, POR will be rendered inactive. Contrary to the Examiner's interpretation, the output POR of buffer 650 is rendered active from activation of a second activated power-on detection signal of the power supply detection signals POR 1 and POR2 until inactivation of a first activated power detection signal of the power supply detection signals POR1 and POR2.

Therefore, the period interpreted by the Examiner in Crotty is of no significance. The first power-on detection circuit 630 or the dual voltage level detection circuit 210 merely detects

the voltage state of first power supply voltage Vcc1 only when second power supply voltage Vcc2 is stable, and is not configured to detect the voltage level of first power supply voltage Vcc1 to produce the power-on detection signal independently of second power supply voltage Vcc2. To put it another way, the active period of power-on detection signal POR is determined by a period until the stabilization of second power supply voltage Vcc2, regardless of the supply situation of first power supply voltage Vcc1, which is different from the period recited in each independent claim.

In this regard, neither scenario suggests the configuration of claim 1, which recites "a main power-on detection circuit...for generating a main power-on detection signal rendered active from activation of a first activated power-on detection signal of the first and second power-on detection signals until inactivation of a second activated power-on detection signal of the first and second power-on detection signals."

* * *

Claim 11 recites "a main power-on detection circuit...for generating a main power-on detection signal rendered active from activation of a first activated detection signal of the internal voltage power-up detection signal and the power-on detection signal until inactivation of second activated detection signal of the internal voltage power-up detection signal and the power-on detection signal."

Claims 19 recites, "a main power-on detection circuit...for activating a main power-on detection signal from activation of a first activated power-up detection signal in the power-up detection signals until inactivation of a last activated power-up detection signal in the power-up detection signals, to hold an internal circuit in a reset state."

Claim 20 recites, "a main power-on detection circuit...made active from activation of a first activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal until inactivation of a last activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal, to hold an internal circuit in a reset state."

In accordance with the detailed explanation above, Crotty also fails to teach the configurations recited by claims 11, 19, and 20, and specifically, the activation period as defined by the claims.

Prior Art Rejections

As to the anticipation rejection of claims 1-3, 7, and 19, Crotty fails to suggest the features of independent claims 1 and 19, as discussed in detail above. Dependent claims 2-3 and 7 are patentable at least based on dependency, and for the other novel configurations recited by the claims. Withdrawal of the rejection is respectfully solicited.

As to the obviousness rejection of claims 11, 16-18, and 20, Crotty fails to suggest the novel features of independent claims 11 and 20, described in detail above. Dependent claims 16-18 are patentable at least based on dependency, and for the other novel configurations recited by the claims.

Further, the Office Action acknowledges that Crotty does not disclose the claimed internal voltage generation circuit of claims 11 and 20, but states that it would have been obvious to use a voltage step-down circuit to generate the reduced voltage. The Office Action goes on to state that it would have been obvious to use the step-down circuit for generating the internal voltage Vcc1..."if the design value of the internal voltage is higher than a voltage level which the circuit provides."

Assuming *arguendo* that the deficiencies of Crotty are curable, it is emphasized that in the application of a rejection under 35 U.S.C. §103, it is incumbent upon the Examiner to factually support a conclusion of obviousness. *In re Mayne,* 104 F.3d 1339, 41 USPQ2d 1451 (Fed. Cir. 1997). The Examiner has not produced any factual support for the assertion that it would have been obvious use the step-down circuit for generating the internal voltage Vcc1.

The Examiner should recognize that the fact that the prior art *could* be modified so as to result in the combination proposed in an effort to meet the claims would not have made the modification obvious unless the prior art suggested the desirability of the modification. *In re Deminski*, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986). The Examiner has failed to factually support and produce any evidence showing a desirability of the modification (motivation). (*emphasis added*). In the absence of such a prior art suggestion for modification of the references, the basis of the rejection is no more than inappropriate hindsight reconstruction using appellant's claims as a guide. *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967).

Accordingly, the Examiner has failed to establish a prima facie case of obviousness of claims 11, 16-18, and 20. Withdrawal of the rejection is respectfully solicited.

New Claims

Claims 21-24 each depend upon independent claims 1, 11, 19, and 20, respectively, and therefore, are allowable at least based on dependent, and for the novel features that the claims recite.

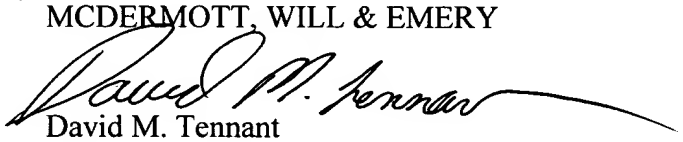
Conclusions

All outstanding issues set forth by the Examiner in the Office Action have been addressed and resolved, as provided for above. Hence, the application stands in a condition for allowance. If the Examiner has any questions concerning this response or the application in general, the Examiner is encouraged to contact the undersigned to expedite allowance of this case.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



David M. Tennant
Registration No. 48,362

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 SAB:DT:edd
Facsimile: (202) 756-8087
Date: February 7, 2003

VERSION SHOWING MARKED-UP CHANGES

Please amend claims 1, 11 and 19 as follows:

1. (TWICE AMENDED) A semiconductor integrated circuit device comprising:

a first power-on detection circuit responsive to a first power supply voltage for detecting power-on of said first power supply voltage to activate a first power-on detection signal according to a result of detection;

a second power-on detection circuit responsive to a second power supply voltage for detecting power-on of said second power supply voltage independently of a voltage level of said first power supply voltage, to activate a second power-on detection signal according to a result of detection, said first power-on detection circuit performing detection of the power-on independently of a voltage level of the second power supply voltage;

a main power-on detection circuit coupled to the first and second power-on detection circuits for generating a main power-on detection signal rendered active from activation of a first activated power-on detection signal of the first and second power-on detection signals until inactivation of a second activated power-on detection signal of the first and second power-on detection signals.

11. (TWICE AMENDED) A semiconductor integrated circuit device comprising;

an internal voltage generation circuit receiving a first power supply voltage and generating, from said first power supply voltage, an internal voltage different in voltage level from said first power supply voltage;

an internal voltage application detection circuit for activating an internal voltage power-up detection signal according to a voltage level of said internal voltage;

a power-on detection circuit for detecting power-on of a second power supply voltage independently of a voltage level of said internal voltage, to activate a power-on detection signal according to a result of detection, said internal voltage application detection circuit performing detection of the voltage level of the internal voltage independently of a voltage level of the second power supply voltage; and

a main power-on detection circuit responsive to said internal voltage power-up detection signal and said power-on detection signal for generating a main power-on detection signal rendered active from activation of a first activated detection signal of the internal voltage power-up detection signal and the power-on detection signal until inactivation of second activated detection signal of the internal voltage power-up detection signal and the power-on detection signal.

19. (TWICE AMENDED) A semiconductor device receiving a plurality of power supply voltages for operation, comprising:

a plurality of power-up detection circuits provided for the respective power supply voltages and detecting power-up of the respective power supply voltages to generate power-up detection signals corresponding to the respective power supply voltages, each power-up detection circuit detecting a voltage level of a corresponding power supply voltage independently of a voltage level of the power supply voltage other than the corresponding power supply voltage; and

a main power-on detection circuit coupled to receive the respective power supply voltages for activating a main power-on detection signal from activation of a first activated power-up detection signal in the power-up detection signals until inactivation of a last activated

power-up detection signal in the power-up detection signals, to hold an internal circuit in a reset state.

20. (TWICE AMENDED) A semiconductor device comprising:

internal voltage generation circuitry coupled to receive at least one power supply voltage and generating, from said at least one power supply voltage, a plurality of internal voltages differing in voltage level from each other [and from said at least one power supply voltage];

internal voltage power-up detection circuitry provided for at least one of the plurality of internal voltages and detecting power-up of the at least one internal voltage in accordance with a voltage level of said at least one internal voltage for generating at least one internal voltage power-up detection signal for said at least one internal voltage;

power-on detection circuitry provided for at least one power source voltage other than said at least one power supply voltage, for detecting power-on of said at least one power source voltage in accordance with a voltage level of said at least one power source voltage independently of the voltage level of said at least one internal voltage, to generate at least one power-on detection signal for the respective at least one power source voltage, said internal voltage power-up detection circuitry performing detection independently of the voltage level of the at least one power source voltage; and

main power-on detection circuitry responsive to said at least one internal voltage power-up detection signal and said at least one power-on detection signal for generating a main power-on detection signal made active from activation of a first activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal until inactivation

of a last activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal, to hold an internal circuit in a reset state.